Remarks

Claims 1-19 are pending in the application.

Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 6,069,516 issued to Vargha on May 30, 2000.

Claims 16-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,821,825 issued to Kobayashi on October 13, 1998.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vargha in view of United States Patent No. 6,028,496 issued to Ko et al. on February 22, 2000.

Each of the various rejections and objections are overcome by amendments which are made to the specification, drawing, and/or claims, as well as, or in the alternative, by various arguments which are presented.

Entry of this Amendment is proper under 37 CFR § 1.116 since the amendment: (a) places the application in condition for allowance for the reasons discussed herein; (b) does not raise any new issue requiring further search and/or consideration since the amendments amplify issues previously discussed throughout prosecution; (c) satisfies a requirement of form asserted in the previous Office Action; (d) does not present any additional claims without canceling a corresponding number of finally rejected claims; or (e) places the application in better form for appeal, should an appeal be necessary. The amendment is necessary and was not earlier presented because it is made in response to arguments raised in the final rejection. Entry of the amendment is thus respectfully requested.

Any amendments to any claim for reasons other than to distinguish such claim from known prior art are not being made with an intent to change in any way the literal scope of such claims or the range of equivalents for such claims. They are being made simply to present language that is better in conformance with the form requirements of Title 35 of the United States Code or is simply clearer and easier to understand than the originally presented language. Any amendments to any claim in order to distinguish such claim from known prior art are being made only with an intent to change the literal scope

of such claim in the most minimal way, i.e., to just avoid the prior art in a way that leaves the claim novel and not obvious in view of the cited prior art, and no equivalent of any subject matter remaining in the claim is intended to be surrendered.

Prior-Art-Based Rejections

With regard to the rejection under 35 U.S.C. 102, the Office Action indicated that applicant's arguments were not persuasive because the limitation of the circuit that is claimed in the independent claims being an active inductor was not recited in the body of the claims but only in the preamble, and the preamble is given no weight toward patentability. Applicant believes that the preamble, as written, should have been given patentable weight in considering the meaning of the claims, and that was the original intent, as can be gathered from the entire specification and the thrust of the heretofore presented arguments. Therefore, without changing the intended subject matter within the scope of the claims, applicant has reworded the independent claims to more clearly recite the limitation that the circuit is arranged to operate as an active inductor. Hence, applicant's independent claims, and all the dependent claims which depend respectively therefrom, are allowable over Vargha and Kobayashi under 35 U.S.C. 102 for the reasons previously set forth in this regard.

With regard to the rejection under 35 U.S.C. 103, the Office Action's statement to the contrary notwithstanding, one would **not** combine Vargha and to Ko et al., and it is clear that one should **not** do so. This is because the biasing regimes of Vargha and Ko et al. are mutually exclusive. One either has Vargha, which is a switch, or Ko et al., which is an active inductor. To do as the Office Action suggests, to insert the resistors of Ko et al. into the circuit of Vargha, is to entirely **ruin** the circuit of Vargha.

It is again noted that the resistors of Ko et al. do **NOT** serve to protect the MOSFET, but to **bias** it for proper operation as an active inductor. The Office Action's suggestion that the resistors serve an additional or alternative function of protection reads nicely and may appear, at first glance seductive in an Office Action, but it is based on a misunderstanding of the circuit in Ko et al. and a complete mischaracterization of the circuit's nature and the function of the resistors. Furthermore, one of ordinary skill in the

art would readily recognize that if he were to try and "protect" the MOSFET of Vargha as suggested by the Office Action, i.e., using the alleged "protection" technique of Ko et al., that doing so would, as indicated, completely ruin the circuit of Vargha. Therefore, one of ordinary skill in the art would **not**, for any considered reason, combine the Vargha and Ko et al. references if merely given the Vargha and Ko et al. references. Hence there is NO rational upon which an obviousness rejection using the Vargha and Ko et al. references can be based.

Since there is no teaching, suggestion, or motivation to combine Vargha with Ko et al., doing so is an improper basis for a rejection, and applicants claims 1-13 are allowable over Vargha and Ko et al. applicant's claims are allowable over the suggested combination.

Conclusion

It is respectfully submitted that the Office Action's rejections have been overcome and that this application is now in condition for allowance. Reconsideration and allowance are, therefore, respectfully solicited.

If, however, the Examiner still believes that there are unresolved issues, he is invited to call applicant's attorney so that arrangements may be made to discuss and resolve any such issues.

In the event that an extension of time is required for this amendment to be considered timely, and a petition therefor does not otherwise accompany this amendment, any necessary extension of time is hereby petitioned for, and the Commissioner is authorized to charge the appropriate cost of such petition to the **Lucent Technologies Deposit Account No. 12-2325**.

Respectfully,

Eduard Sackinger

By Eugene J. Rosenthal

Eugene J. Rosenthal, Attorney
Reg. No. 36,658
732-949-1857

Lucent Technologies Inc.

Date: Oct. 22, 2002

MARKED-UP VERSIONS OF THE AMENDED CLAIMS

IN THE CLAIMS

Unchanged claim 1

1. ~~An active inductor~~ A circuit for use as an active inductor on an integrated circuit having a power supply voltage supplied ~~from~~ at a first power supply terminal, comprising:

an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to said power supply voltage and said source terminal being one of the terminals of said active inductor; and

a resistor having a first terminal coupled to said gate terminal and a second terminal coupled to a voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied at ~~by~~ said first power supply terminal and the same sign as said power supply voltage;

said circuit being adapted so that when said circuit is operating said circuit behaves as an active inductor between said source terminal and an other terminal of said active inductor on said integrated circuit.

Replacement claim 2

2. The invention as defined in claim 1 wherein ~~the~~ other ~~one of the~~ terminals of said active inductor is said first power supply terminal.

Unchanged claim 3

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

Unchanged claim 4

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 5

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 6

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

Unchanged claim 7

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

Unchanged claim 8

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

Unchanged claim 9

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

Unchanged claim 10

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

Unchanged claim 11

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

Unchanged claim 12

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Unchanged claim 13

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Replacement claim 14

14. (Amended) A~~n~~ circuit for use as an active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a beyond voltage generator which generates a beyond voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and ~~so that~~ said MOS transistor is adapted to operate~~s~~ as said active inductor.

Replacement claim 15

15. (Amended) The invention as defined in claim 14 wherein said beyond voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said beyond voltage generator.

Replacement claim 16

16. (Amended) An ~~active inductor on an~~ integrated circuit~~, said active inductor~~ comprising a metal oxide semiconductor (MOS) transistor ~~that~~ adapted to operate~~s~~ as ~~said~~ an active inductor ~~and being characterized in~~ that ~~said active inductor~~ is biased using a voltage generated on said integrated circuit that is outside the range of the voltage supplied by a power supply off of said integrated circuit for operating said integrated circuit.

Unchanged claim 17

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 18

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 19

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.